What is claimed is:

1. A method of forming semiconductor device, said method comprising the steps of:

providing a first conductive type semiconductor substrate having an epi-layer doped with impurities of said first conductive type formed thereon;

forming a hard mask on said epi-layer;

patterning said semiconductor substrate by using said hard mask as an etching mask to form first trenches at a core region and termination trench at a border region of said semiconductor substrate;

performing ion implant to form a first-type doping region beneath bottoms of said first trenches and said termination trench;

depositing an undoped silicon layer on all areas till said first trenches are filled in and over a level of said hard mask to a predetermined thickness;

forming a thermal oxide layer by performing a thermal oxidation to oxidize those portions of silicon layer out of said first trenches;

defining an active region and a termination region by patterning said hard mask and said thermal oxide layer;

forming a barrier metal layer on said active region and said thermal oxide layer;

performing an anneal step to form a metal silicide layer on said active region;

forming a top metal layer on said metal silicide layer and said barrier metal layer;

patterning said top metal layer to define an anode electrode;

performing a chemical polishing process to remove backside layers formed in previously step till said semiconductor substrate is exposed and thinned; and

forming a cathode electrode on a backside surface of said semiconductor substrate.

2. The method according to Claim 1 wherein said hard mask is a stack layer formed of a first oxide layer, a nitride layer, and a second oxide layer having a thickness between about 5 to 100 nm, 50-300 nm, and 0 to1000 nm.

3. The method according to Claim 1 wherein said first-type doping region is formed by implanting B^+ or BF_2^+ ion species or both.

4. The method according to Claim 1 wherein said silicon layer is a polycrystalline silicon layer or an amorphous silicon layer.

5. The method according to Claim 1 wherein said barrier metal layer is made of material selected from the group consisting of Al, AlCu, AlSiCu, Ti, Ni, Cr, Mo, Pt, Zr, Co, W, Ti/TiN and the combination thereof.

6. The method according to Claim 1 after a step of performing an anneal step to form a metal silicide layer further comprises a step of un-reacting metal layer removal.

7. The method according to Claim 1 wherein said top metal layer is formed of stacked layers of Al, AlCu, AlSiCu, Ti/Ni/Ag.

8. The method according to Claim 1 wherein said hard mask is a stack layer, from said epi-layer sequentially, formed of a first oxide layer, a nitride layer, and a second oxide layer having a thickness between about 5 to 100 nm, 50-300 nm, and 0 to1000 nm.

9. The method according to Claim 1 wherein said active region is an area includes all of said first trenches, and said anode electrode is over said active region extended to cover a portion of said termination trench.

10. The method according to Claim 1 wherein said active region is an area includes all but the outermost one of said first trenches at both terminals from a cross-sectional view, and said anode electrode is over said active region.

11. The method according to Claim 1 wherein said hard mask is an oxide layer.

12. The method according to Claim 1 after a step of performing ion implant further comprises the step of:

removing said hard mask;

forming a thermal oxide lining layer on sidewalls of said first trenches and said termination trench to recover etching damage;

depositing a silicon layer on all areas till said first trenches are filled in and over a predetermined thickness;

forming a thermal oxide layer by performing a thermal oxidation to oxidize those portions of silicon layer outside said first trenches;

defining an active region and a termination region by patterning said hard mask and said thermal oxide layer;

forming a barrier metal layer on said active region and said thermal oxide layer;

performing an anneal step to form a metal silicide layer on said active region;

forming a top metal layer on said metal silicide layer and said barrier metal layer;

patterning said top metal layer to define an anode electrode;

performing a chemical polishing process to remove backside layers formed in previously step till said semiconductor substrate is exposed and thinned; and

forming a cathode electrode on a backside surface of said semiconductor substrate.

13. The method according to Claim 12 wherein said thermal oxide lining layer having a thickness between about 10 to 1000 nm.

14. A power rectifier device, comprising :

an n+ substrate having a n-drift layer formed thereon;

a cathode metal layer formed on a surface of said n+ substrate opposite said n-drift layer;

an active region having a metal silicide layer formed thereon;

a termination region being defined at positions outer of said active region;

an insulating layer formed on said n-drift layer and on said termination region;

four first trenches along a line and filled with an un-doped polycrystalline silicon layer spaced from each other and the second and the third of said trenches formed into said n- drift layer of said substrate, and the first and the fourth of said trenches formed into said insulating layer and said n- drift layer of said substrate;

said active region being defined from a first interval to a second interval, wherein said first interval is in between the first one and the second one of said first trenches, and said second interval is in between the third one and the fourth one of said first trenches;

a thermal oxide layer formed on said termination region;

an anode electrode formed on metal silicide layer and extended to cover the first and the fourth of said first trenches.

15. The power rectifier device according to Claim 14 wherein said active region further comprises the first and the fourth of said trenches, so that said insulting layer formed thereon is removed and thus said metal silicide layer is formed over four first trenches and said anode electrode is formed extended to cover a portion of said termination trenches.

16. The power rectifier device according to Claim 14 wherein said insulating layer is a stack layer, from said epi-layer sequentially, formed of a first oxide layer, a nitride layer, and a second oxide layer having a thickness between about 5 to 100 nm, 50-300 nm, and 0 to1000 nm.

17. The power rectifier device according to Claim 14 wherein said insulating layer is an oxide layer.

18. The power rectifier device according to Claim 14 further comprises an oxide lining formed on a sidewall and bottom of said four first trenches and said termination trenches.

19. The power rectifier device according to Claim 6 wherein said anode electrode is a layer selected from Al, AlCu, AlSiCu or a stack layer formed of Ti, Ni, and Ag.